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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,552	09/19/2003	Thomas R. Apel	TRQ-12893	5545

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BEVER HOFFMAN & HARMS, LLP
TRI-VALLEY OFFICE
1432 CONCANNON BLVD., BLDG. G
LIVERMORE, CA 94550

EXAMINER	
SHINGLETON, MICHAEL B	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/666,552	APEL ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 11/10/2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 6-14, 16, 17 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. 5,162,756 (Taniguchi) in view of Holt.

Figure 2 of Taniguchi discloses a power amplifier circuit. Note that the goal of these circuits of Taniguchi is to "obtain a high power high frequency signal" (See column 3, around line 59) and thus these circuits are power amplifier circuits. Taniguchi includes a first amplifier FET_1 that is configured to receive an input signal that is the unmarked signal at the node that directly connects elements L_1, L_3, and L_4. Note that the first amplifier receives this signal through element L_3. This is only giving the broadest reasonable interpretation to the claims consistent with the specification. See MPEP 904.01. The first amplifier clearly provides a "first" output signal. Element L_4 of Taniguchi is a first delay element that introduces a delay to the input signal and applies this to the input of a "second" amplifier FET_2. This second amplifier clearly has an output signal and provides a "first" delayed output signal to the node directly connecting elements L_3', L_4' and L_1'. The top of page 9, of applicant's specification clearly sets forth that an impedance inverter can be a quarter wavelength transmission line. Thus all the quarter wavelength lines of Taniguchi are "impedance inverters" as set forth by applicant and is in accordance with applicant's application. These impedance inverters of Taniguchi are in accordance with applicant's specification provides the "impedance inversion". The claimed functions of exhibiting a first and second "impedance optimum load" and exhibiting a characteristic impedance equal to the first impedance are all inherent in the impedance inverter combined with these amplifiers because the impedance inverter is the same structure as disclosed and claimed (See above.). Thus the impedance/delay element L_3'also introduces a second delay to the first output signal thereby creating a second delayed output signal. The node directly connecting elements L_3', L_4' and L_1' and the node directly connecting elements L_5', L_6' and L_2' in combination with the node that directly connects elements L_1' and L_2' provides the means for combining the first and second delayed output signals that ultimately provides the high frequency amplified output signal S_{out}. This output signal is provided on the output terminal "P_1' ". Note that FET_3

of Taniguchi is a third amplifier that is configured to receive an input signal and in response provide a second output signal. Element L_5' of Taniguchi provides a third delay circuit that is configured to introduce the second delay to the second output signal thereby creating a third delayed output signal. The combining means mentioned above also combines the third delayed output signal with those mentioned above to ultimately form the output signal. Taniguchi is silent on showing the bias circuit or what applicant calls "a bias control circuit" that biases the first and second amplifiers to operate in the linear range, i.e. class A, AB or B. Applicant should note that while Taniguchi is silent on the bias circuit, as is known to those of ordinary skill in the art, Taniguchi inherently must have a bias circuit because this is a necessary circuit needed so that the amplifier(s) can operate. Taniguchi is also silent on the first amplifier being composed of a first set of transistors and the second amplifier being composed of a second set of transistors.

The structure indicated above clearly provides for the claimed method of the claims indicated at the beginning of this rejection except for as indicated above Taniguchi is silent on providing a bias control circuit that biases the amplifiers such that linear operation is obtained.

It is well known to compose use multiple transistors connected in parallel for a single transistor. These are art recognized equivalent structures. Using multiple transistors connected in parallel has the additional advantage of higher current handling capability over a single transistor amplifier employing the same transistor as the individual transistors of the parallel combination. Accordingly it would have been obvious to replace the single transistors of Taniguchi with a parallel combination of transistors. One of ordinary skill in the art would have been motivated to do so because these are art recognized equivalent structures and the parallel combination of transistors has the added advantage of larger current handling capability as is well known in the art.

Holt teaches that it is well known to provide a bias circuit so that the amplifier can operate, i.e. amplify and to choose the bias level, so that a linear operation is obtained. Linear operation is a measurement of how accurately the amplifier reproduces an input signal multiplied by a gain ideally S_{out} $=S_{in}$(Gain). Thus, the selection of the class of operation is merely the selection of a result effective variable that determines how accurate the amplifier follows the input signal

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Taniguchi with a bias control circuit(s) that biases the first and second amplifiers such that linear operation is obtained for these amplifiers because, as the reference is silent on the exact biasing circuit one of ordinary skill in the art would have been motivated to use any conventional art recognized equivalent biasing circuit therewith such as the class A, AB or B biasing

circuits of Holt. In addition, one of ordinary skill would have been motivated to do so because providing a bias circuit to cause operation in the linear region, i.e. Class A, AB or B, has the added advantage of providing the most accurate amplification of the input signal as taught by Holt. Note that the claims must be given the broadest reasonable interpretation consistent with the specification. The two bias voltages, one for the first amplifier and one for the second can be the same voltage. Thus, reciting the first voltage to a first subset of the first set of transistors... is an obvious consequence of the combination made obvious above.

Claims 4, 5, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. 5,162,756 (Taniguchi) in view of Holt as applied to claims 1, 3, 6-14, 16, 17, 20-22 above, and further in view of Kim et al. 6,617,929 (Kim).

All the reasoning as applied in the rejection of claims 1, 3, 6-14, 16, 17, 20-22 and the following: Taniguchi is silent on the use of a preamplifier or "input amplifier stage". It is well known and common knowledge to provide multiple stages of amplification so as to provide a large overall amplification factor with smaller amplifiers or stages. It is also well known to do so to provide for improved linear operation. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a preamplifier or "input amplifier stage" so as to "spread out" the amplification factor, i.e. use less expensive amplifiers to obtain the same gain as more expensive amplifier and additionally provide for better linear operation as is well known in the art.

Kim teaches that it is well known to provide impedance matching circuits just prior to an amplifier and just after an amplifier. Impedance matching circuits are well known to be used to match impedance, i.e. they allow for maximum power transfer and minimum reflections. Note that the impedance matching circuits, i.e. load matching and input matching, are between the delay lines and the amplifiers thereby providing the best possible match to these lines and amplifiers.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to placed impedance matching circuits just prior and just after the amplifiers of Tanichuchi. One of ordinary skill would have been motivated to do so that a maximum power transfer and minimum reflection can be obtained as taught by Kim.

Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taniguchi et al. 5,162,756 (Taniguchi) in view of Holt as applied to claims 1, 3, 6-14, 16, 17, 20-22 above, and further in view of Cheng et al. 2002/0190790 (Cheng).

All the reasoning as applied in the rejection of claims 1, 3, 6-14, 16, 17, 20-22 and the following: Taniguchi fails to describe using the biasing arrangement to disable one or more of the amplifiers in accordance with the power level one wants to obtain.

Cheng teaches that one can selectively supply the bias voltages each of the parallel-connected amplifiers so as to control the operation of these amplifiers, i.e. whether they are on or off. This controls the amount of power delivered to the load (See page "4" paragraph numbered "[0037]".),

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the bias control circuit of Taniguchi in view of Holt selectively control the bias voltages to the respective amplifiers of the arrangement. One of ordinary skill would have been motivated to do so as to control the amount of output power as taught by Cheng.

Response to Arguments

Applicant's arguments filed 11-10-2004 have been fully considered but they are not persuasive. Applicant states that the examiner stated that Tanaguchi does not disclose a bias control circuit. The actual statement from the examiner is that Tanaguchi is silent on the bias circuit. This means that there could be one but it is not shown. Applicant should ~~allow~~ also note that a bias circuit can mean a supply source and that all such circuits are a bias control circuit, for they all control i.e. set the bias. Applicant also disagrees with the examiner that Tanaguchi inherently has a bias control circuit. The examiner respectfully disagrees for all transistor amplifiers must have a bias control circuit in order to operate i.e. be enabled. Thus the examiner has set forth that Tanaguchi does disclose a bias control circuit, Tanaguchi is just silent in the exact mentioning of this circuit. Applicant also states that the Tanaguchi or Tanaguchi in view of Holt does not teach or suggest "a bias control circuit configured to provide a first bias voltage that enables the first amplifier and causes the first amplifier to operate in a linear mode...". The examiner respectfully disagrees. There must be a bias control circuit so that the transistor amplifiers are enabled and the selection of the bias selects the class of operation especially if bi-polar transistors are used. Applicant has not provided any evidence that the transistor amplifiers of Tanaguchi in view of Holt would not operate in a linear manner. A linear manner in transistors is common known to mean a substantially linear manner over a certain range for no transistor is strictly linear.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770. The examiner can normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Mondays. The examiner normally has the second Mondays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
Jan 21, 2005

MICHAEL B SHINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817